20th HiPEAC Workshop on
Reconfigurable Computing (WRC 2026)
January 27th, 2026

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João M. P. Cardoso, *University of Porto, Portugal*

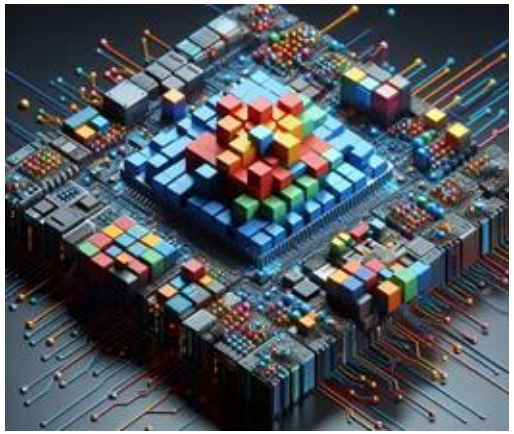
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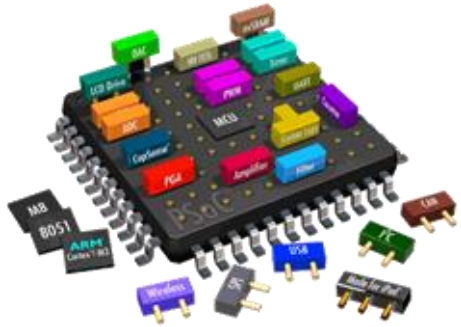
* "Reconfigurable Computing concept", Made with Designer. Powered by DALL·E 3.

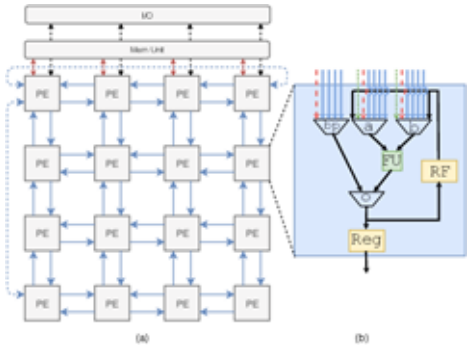
HiPEAC Conference: January 26-28, 2026, Krakow, Poland

www.fe.up.pt/wrc2026

WRC topics over the years







2020
- Open source FPGAs
- FPGAs in space

2021
- Smart, adaptive and reliable systems
- Reconfigurable computing as reboot technology in SoC world

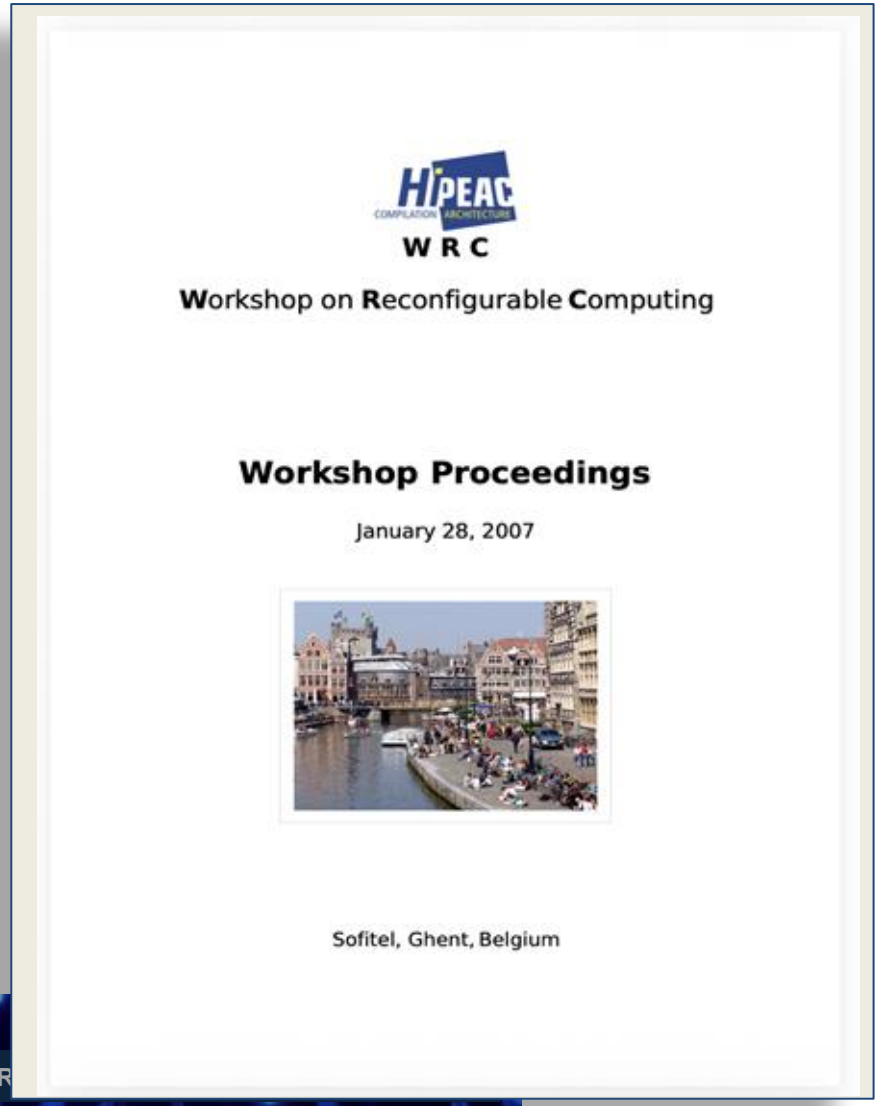
2022
- Recent research on Coarse-Grained Reconfigurable Arrays (CGRAs)
- Open-source initiatives of High-Level Synthesis (HLS) for FPGAs
- The use of FPGAs for accelerating Graph-Algorithms
- The role of FPGAs for Artificial Intelligence (AI)

2023
- Using Reconfigurable Computing for Artificial Intelligence (AI)
- Software Stacks for Reconfigurable Computing)
- Dynamic reconfigurable and runtime adaptable RC approaches
- Reconfigurable Computing for Fault-Tolerant Application
- Open-source initiatives for RC (FPGA fabrics, CGRAs, tools)

2024
- Open-source initiatives for RC (FPGA fabrics, CGRAs, tools)
- The use of FPGAs for accelerating Graph-Algorithms
- The role of FPGAs in Artificial Intelligence (AI)
- FPGAs as overlays for non-conventional computing
- Dynamic reconfigurable and runtime adaptable RC approaches

2025
- Recent research on Coarse-Grained Reconfigurable Arrays (CGRAs)
- Open-source initiatives for RC (FPGA fabrics, CGRAs, tools)
- The use of FPGAs for accelerating Graph-Algorithms
- The role of FPGAs in Artificial Intelligence (AI)
- FPGAs as overlays for non-conventional computing
- Dynamic reconfigurable and runtime adaptable RC approaches

20 years of WRC



Organizing Committee

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WRC 2026 Topics

- **Open-source** initiatives for RC (FPGA fabrics, CGRAs, tools)
- Adaptive HPC and **Reconfiguration**
- **Reconfigurable** Architectures for Real-Time Vision Systems

Programme

CET	Morning Session
10:00 - 10:05	*Opening address of WRC*
10:05 - 11:00	Keynote: **Accelerating ML for Science with Open Source Tools** Prof. Seda Ogrenci, Northwestern University, USA
11:00 - 11:30	***Coffee break***
11:30 - 12:00	**Adaptive HPC & Accelerator Integration - Reliability, Deployment & AI Issues** Prof. Jürgen Becker, Karlsruhe Institute of Technology, Germany
12:00 - 12:30	**Partial Reconfiguration in FABulous FPGAs** Prof. Dirk Koch, Heidelberg University, Germany
12:30 - 13:00	**Microreconfiguration for circuit specialisation on the configuration bit level** Prof. Dirk Stroobandt, Ghent University, Belgium
13:00 - 14:00	***Lunch***

	Afternoon Session
14:00 - 15:00	**A Long-Term Perspective on Reconfigurable Architectures for Real-Time Vision Systems - from Convolutional Filtering to Graph Neural Networks.** Prof. Marek Gorgon & Dr Tomasz Kryjak, AGH University of Krakow, Poland
15:00 - 15:30	**Ubitium: Dynamically switching a CGRA between RISC-V OoO CPU and Data-Flow Accelerator Modes** Dr Lars Bauer, Sebastian Ottlik Ubitium GmbH
15:30 - 16:00	***Coffee break***
16:00 - 16:30	***PhD Forum***
16:30-17:00	**(Almost) 100%** Dr Martin Langhammer, ALTERA
17:00-17:30	***Round-Table discussion***
17:30	***Closing of the workshop***



7 invited talks + PhD forum + round-table discussion

Session 1

10:05 - 11:00	**Accelerating ML for Science with Open Source Tools** Prof. Seda Ogrenci, Northwestern University, USA



Panel discussion. 17:00- (open)

Main topic:

RC in the Age of AI, RISC-V, OpenSource, Accelerators & Chiplets: Lessons Learned & Next Steps?

***Participants**:*

- Seda Ogrenci, Northwestern University, USA
- Cristina Silvano. Polimi, Italy
- Marek Gorgon, AGH University of Krakow, Poland
- Lars Bauer, Ubitium GmbH, Germany
- Martin Langhammer, Altera, UK

Chair: Juergen Becker, *KIT, Germany*

Closing Session

A big thank you
to all attendees, speakers, and
to the HiPEAC'2026 organizing committee

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