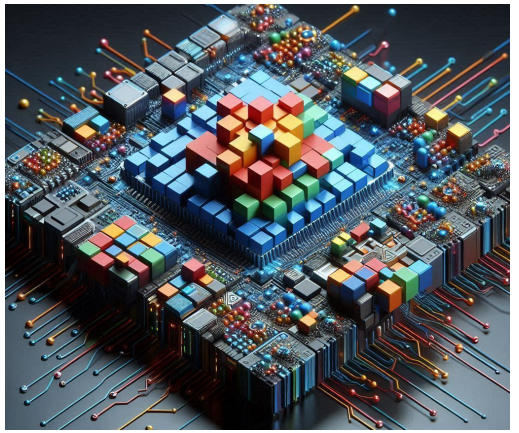
# 19th HiPEAC Workshop on
# Reconfigurable Computing (WRC 2025)
## January 21st, 2025

**General Chairs**
Juergen Becker, *KIT, Germany*
João M. P. Cardoso, *University of Porto, Portugal*

**Technical Program Chairs**
Christos-Savvas Bouganis, Imperial College London, UK
Vanderlei Bonato, ICMC/USP, Brazil

**Local Chair**
Carlos Alvarez, Barcelona Supercomputing Center, Spain



* "Reconfigurable Computing concept", Made with Designer. Powered by DALL·E 3.

**HiPEAC Conference: January 20-22, 2025, Barcelona, Spain**

**www.fe.up.pt/wrc2025**

# WRC topics over the years

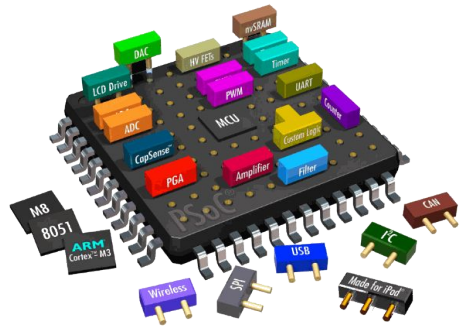



**2020**

- Open source FPGAs
- FPGAs in space

**2021**

- Smart, adaptive and reliable systems
- Reconfigurable computing as reboot technology in SoC world

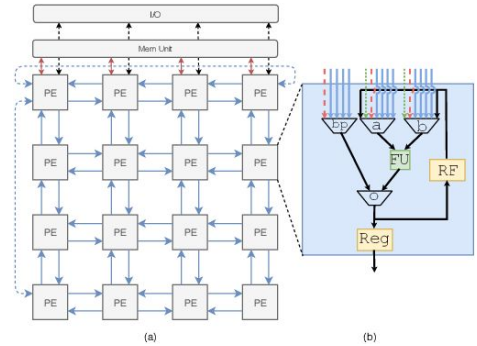



**2022**

- Recent research on Coarse-Grained Reconfigurable Arrays (CGRAs)
- Open-source initiatives of High-Level Synthesis (HLS) for FPGAs
- The use of FPGAs for accelerating Graph-Algorithms
- The role of FPGAs for Artificial Intelligence (AI)

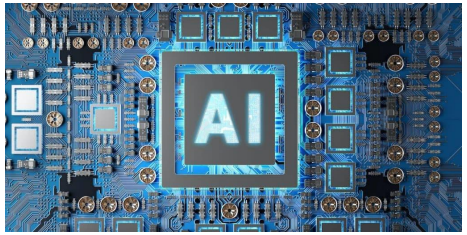
**2023**

- Using Reconfigurable Computing for Artificial Intelligence (AI)
- Software Stacks for Reconfigurable Computing)
- Dynamic reconfigurable and runtime adaptable RC approaches
- Reconfigurable Computing for Fault-Tolerant Application
- Open-source initiatives for RC (FPGA fabrics, CGRAs, tools)




**2024**

- Open-source initiatives for RC (FPGA fabrics, CGRAs, tools)
- The use of FPGAs for accelerating Graph-Algorithms
- The role of FPGAs in Artificial Intelligence (AI)
- FPGAs as overlays for non-conventional computing
- Dynamic reconfigurable and runtime adaptable RC approaches



# WRC 2025 Topics

- Recent research on Coarse-Grained Reconfigurable Arrays (CGRAs)
- Open-source initiatives for RC (FPGA fabrics, CGRAs, tools)
- The use of FPGAs for accelerating Graph-Algorithms
- The role of FPGAs in Artificial Intelligence (AI)
- FPGAs as overlays for non-conventional computing
- Dynamic reconfigurable and runtime adaptable RC approaches

# Programme

| CET | |
|---|---|
| | **Session 1, Chair: Christos Bouganis** |
| 10:00 - 10:05 | Opening address of WRC<br>Juergen Becker, Christos Bouganis, Joao Cardoso |
| 10:05 - 11:00 | **Keynote**: The Next Wave of HLS: Fully Automated PyTorch-to-Accelerator Design Flow for FPGAs<br>Prof. Deming Chen, University of Illinois Urbana-Champaign |
| 11:00 - 11:30 | **Coffee break** |
| | **Session 2, Chair: Christos Bouganis** |
| 11:30 - 12:00 | Optimising Diverse Accelerator Designs<br>Prof. Wayne Luk, Imperial |
| 12:00 - 12:30 | FPGAs to assess the vulnerability of neural network models running at the edge<br>Prof. Theocharis Theochariides, University of Cyprus |
| 12:30 - 13:00 | The SPARKLE RISC-V Overlay ecosystem for Datacenter FPGAS<br>Dr.. Riadh Ben Abdelhamid, Heidelberg University |
| 13:00 - 14:00 | **Lunch** |
| | **Session 3, Chair:João M. P. Cardoso** |
| 14:00 - 14:30 | Multi-FPGA multi-core overlay architectures for executing graph-based applications<br>Prof. David Thomas, University of Southampton |
| 14:30 - 15:00 | HashGrid: Optimized FPGA Architecture for Accelerating Graph Processing in Large-Scale Computing<br>Prof. Roberto Giorgi, University of Siena |
| 15:000 - 15:30 | Omps2@fpga + IMP/OMPIF: Dataflow execution model exploitation with inter-node acceleration<br>Prof. Daniel Jiménez-González, Polytechnic University of Catalonia |
| 15:30 - 16:00 | **Coffee break** |
| | **Session 4, PhD Forum, Chair: João M. P. Cardoso** |
| 16:00 - 16:30 | 6 PhD talks |
| 16:30 - 17:00 | Scalable and Reconfigurable Computing Architectures for AI<br>Diana Goehringer, TU Dresden |
| 17:00 - 17:30 | **Session 5, Round-Table discussion, Chair: Juergen Becker**<br>***RC in the Age of RISC-V, OpenSource and Chiplets: Chances & Challenges*** |
| 17:30 | **Closing of the workshop** |




***8 invited talks + PhD forum + round-table discussion***

# Panel discussion. 17:00- (open)

Main topic:

**RC in the Age of RISC-V, OpenSource and Chiplets: Chances & Challenges**

***Participants:***

- Deming Chen
- Roberto Giorgi
- David Thomas
- Theocharis Theocharides
- Diana Göhringer

**Chair**: Juergen Becker, *KIT, Germany*

# Session 1

10:05 - 11:00 The Next Wave of HLS: Fully Automated PyTorch-to-Accelerator Design Flow for FPGAs
Prof. Deming Chen, University of Illinois Urbana-Champaign



# Closing Session

A big thank you to all attendees, speakers, and to the HiPEAC'2025 organizing committee

- **General Chairs**
  - Juergen Becker, KIT, Germany
  - João M. P. Cardoso, University of Porto, Portugal
- **Program Chairs**
  - Christos-Savvas Bouganis, Imperial College London, UK
  - Vanderlei Bonato, ICMC/USP, Brazil
- **Local Chairs**
  - Carlos Alvarez, Barcelona Supercomputing Center, Spain
- **Web Chair**
  - João Bispo, University of Porto, Portugal
- **Publicity Chairs**
  - Kevin Martin, Université de Bretagne-Sud, France
  - Theocharis Theocharides, University of Cyprus, Cyprus

# Organizing Committee

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