Programme
16th HiPEAC Workshop on Reconfigurable Computing

Monday, June 20th, 2022

CET	**Morning Session**
10:00 - 10:05	Opening address of WRC
10:05 - 10:30	Prof. Dirk Koch, Heidelberg University *Using the FABulous eFPGA Framework for Implementing AI Systems*
10:30 - 11:00	Prof. Roberto Giorgi, University of Siena *Distributed Large-Scale Graph-Processing on FPGAs*
11:00 - 11:30	*Coffee break*
11:30 - 12:00	Prof. Holger Fröning, Heidelberg University *TBA*
12:00 - 12:30	Dr George Lentaris, National Technical University of Athens *The role of FPGAs for enabling onboard AI in space applications*
12:30 - 13:00	Fareed Mohammad Qararya, Chalmers University of Technology *A hybrid FPGA accelerator for MobileNets*
13:00 - 14:00	*Lunch*
	Afternoon Session
14:00 - 14:30	Prof. Martin Margala, University of Louisiana at Lafayette *Optimizing Open Source Toolchain for FPGA bitstream generation*
14:30 - 15:00	Prof. Kevin Martin, Université Bretagne-Sud *Ultra-low Power Computing with CGRAs: an architecture, compilation, and application triptych*
15:00 - 15:30	Kaspar Matas, University of Manchester *Compiling and Operating Dynamic Stream Processing Pipelines on FPGAs*
15:30 - 16:00	*Coffee break*
16:00 - 16:30	Jianiy Cheng, Imperial College London *DASS: An Automated HLS Tool that Combines Dynamic & Static Scheduling*
16:30 - 17:00	*Round-Table discussion*
17:00	Closing of the workshop