10TH INTERNATIONAL SYMPOSIUM ON APPLIED RECONFIGURABLE COMPUTING (ARC 2014)

14-16 APRIL 2014, VILAMOURA, ALGARVE, PORTUGAL

Conference Guide

www.fe.up.pt/arc2014

http://www.arc-symposium.org/

Notes:

Welcome Message

Reconfigurable computing technologies offer the promise of substantial performance gains over traditional architectures via customizing, even at runtime, the topology of the underlying architecture to match the specific needs of a given application. Contemporary configurable architectures allow for the definition of architectures with functional and storage units that match in function, bit-width and control structures the specific needs of a given computation. The flexibility enabled by reconfiguration is also seen as a basic technique for overcoming transient failures in emerging device structures.

The International Symposium on Applied Reconfigurable Computing (ARC, http://www.arc-symposium.org/) aims to bring together researchers and practitioners of reconfigurable computing with an emphasis on practical applications of this promising technology. ARC 2014 is the 10th edition of the symposium and takes place on April 14-16, 2014, in Vilamoura, Algarve, Portugal. The previous editions of ARC took place in Carvoeiro, Algarve, Portugal (ARC'05), Delft, The Netherlands (ARC'06), Mangaratiba. Rio de Janeiro, Brazil (ARC'07), London, UK (ARC'08), Karlsruhe, Germany (ARC'09), Bangkok, Thailand (ARC'10), Belfast, UK (ARC'11), Hong Kong, People's Republic of China (ARC'12), and Marina del Rey, California, USA (ARC'13). ARC 2014 is being organized by the Faculty of Engineering of the University of Porto with the collaboration of the University of Algarve.

Similarly to the first edition of ARC, this year the Portuguese event on Reconfigurable Systems (REC) will take place in Algarve in the day before ARC. We hope that having the two events co-located allows the Portuguese community with interests on reconfigurable hardware to network and discuss ideas with the ARC participants.

We received 57 paper submissions for ARC'2014. The submissions came from 27 countries: USA, UK, Slovakia, Spain, Sweden, The Netherlands, Norway, Pakistan, Poland, Portugal, Qatar, Japan, Republic of Korea, India, Ireland, Australia, Austria, Belgium, Brazil, Canada, People's Republic of China, Cyprus, Denmark, Egypt, Finland, France, and Germany. Each paper was reviewed by at least three members of the program committee. Nine papers had three reviews, forty seven had four reviews, and one paper had five reviews. As a result of the reviewing process, we accepted 16 as regular papers (28.07% of acceptance rate) and 18 as short papers (a global acceptance rate of 59.65%). Selected papers will be invited to submit an ex-

tended version for consideration for a special issue of the ACM Transactions on Reconfigurable Technology and Systems (TRETS) journal. We would like to acknowledge Steve Wilton and David Thomas for their support.

In addition to the oral and poster presentations of the 34 papers, the symposium program includes invited presentations from prestigious speakers, as well as three special sessions focusing on: EU funded projects related to reconfigurable technology, the FP7 EU-funded ALMA project, and on remote FPGA lab environments.

This year we have the pleasure and honor to host Giovanni De Micheli, from EPFL, Switzerland, as our keynote speaker, and David Thomas, from Imperial College, UK, and Giulio Corradi, from Xilinx Inc., Munich, Germany, as our invited presenters from academia and industry, respectively. We would like to express our gratitude for their presence.

We appreciate the support given by Alfred Hofmann, Vice-President Publishing Computer Science, from Springer International Publishing AG, and Anna Kramer, from Springer Computer Science Editorial.

We also would like to acknowledge the authors, the ARC'2014 steering and program committee members, the external reviewers, and all the colleagues participating in the organization of the symposium. Special thanks go to Gabriel Coutinho for his hard work and dedication as proceedings chair. Gabriel extensively reviewed all the papers regarding the LNCS style and worked with the authors on the required modifications.

We hope you enjoy the symposium, have fruitful and inspiring discussions, have time to network, and have some moments of relax.

Welcome to ARC 2014, the 10th Anniversary of the International Symposium on Applied Reconfigurable Computing, and to Vilamoura in Algarve, Portugal. "Algarve. Europe's most famous secret!"

João M.P. Cardoso
Universidade do Porto, Portugal (jmpc@acm.org)

Koen Bertels
Delft University of Technology, The Netherlands (k.l.m.bertels@tudelft.nl)
(ARC 2014 General Co-Chairs)

Diana Goehringer
Ruhr-University Bochum (RUB), Germany (Diana.Goehringer@ruhr-uni-bochum.de)

Marco Santambrogio
Politecnico di Milano, Italy (marco.santambrogio@polimi.it)
(ARC 2014 Program Co-Chairs

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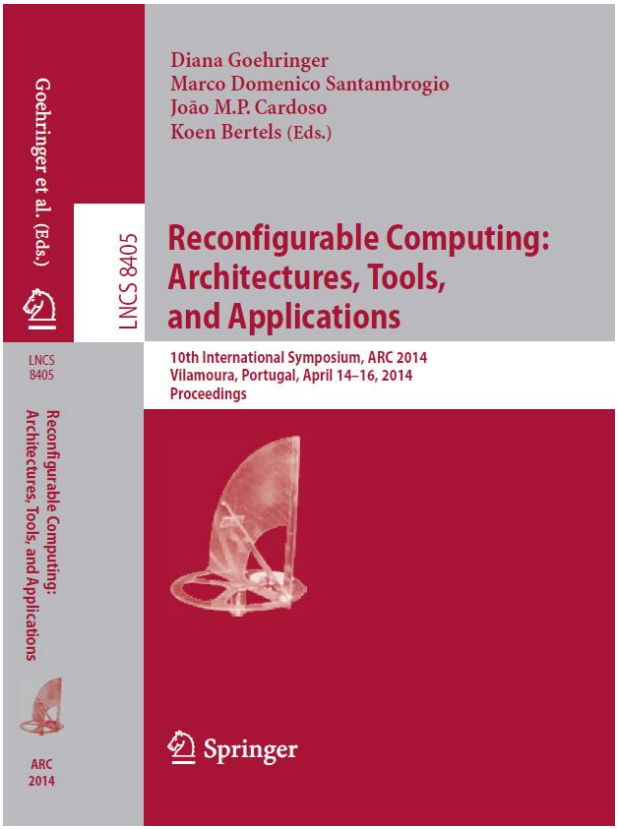
Proceedings

Springer Lecture Notes in Computer Science, LNCS 8405, volume inside the conference bag.



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In memory of Stamatis Vassiliadis [1951-2007], ARC2006-2007 steering committee member

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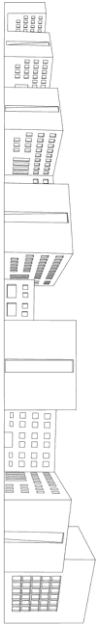
Schedule

Sunday-Thursday, April 13-17, 2014



		Crowne Plaza			Crowne Plaza		Crowne Plaza		Crowne Plaza		Crowne Plaza
		April 13 Sunday		April 14 Monday		April 15 Tuesday		April 16 Wednesday		April 17 Thursday	
		Room Sotavento 3	Room Sotavento 2	Room Sotavento 1		Room Sotavento 1	Room Sotavento 2	Room Sotavento 1		Room Sotavento I	
9:00	-	Registration		Registration		Registration		Registration		Registration	
9:15	10:30		REC'2014	Keynote #1		Keynote #2		Keynote #3		Hands-on: Online Learning, Assessment and Prototyping of Digital Systems using Remote Reconfigurable	
10:30	11:00		Coffee-Break +	Coffee-Break + Poster Session PS1		Coffee-Break + Poster Session PS2		Coffee-Break + Poster Session PS3		Coffee-Break + Poster Session PS1	
11:00	12:30		REC'2014	M1		T1 EU-Funded Projects		W1		Hands-on: eDiViDe: a remote learning platform for FPGA design	
12:30	14:00		Lunch	Lunch		Lunch		Closing Session and Best Paper Award			
14:30	15:45		REC'2014	M2		T2		Lunch			
15:45	16:15		Coffee-Break +	Coffee-Break		Coffee-Break + Poster Session (EU funded projects)		Break			
16:15			REC'2014	M3		AIMA Project	Remote FPGA Lab Environements	Social Event (Boat Cruise, depending on the weather)			
17:30	18:00	Registration									
18:00	19:30	Welcome Cocktail (Sea Front or Caravela Bar)		Break		Break					
				Barbecue (Sea Front or Banquetes room)		Gala Dinner (Banquetes Room)					

REC'2014: *Jornadas de Sistemas Reconfiguráveis* (National Workshop on Reconfigurable Systems)

Overall Program

Sunday, April 13

17:30 - 19:00	**Registration**
18:00 - 19:30	**Welcome Cocktail at the Crowne Plaza Vilamoura Hotel**

Monday, April 14

08:00 - 08:40	**Registration**
08:40 - 09:00	**Welcome Session**
09:00 - 10:00	**Keynote Speaker:** **Technologies and Platforms for Cyberphysical Systems** *Giovanni De Micheli, from EPFL, Switzerland* Chair: Marco Santambrogio, Politecnico di Milano, Italy
10:00 - 10:45	**Coffee Break and Poster Session #1**
10:45 - 12:30	**Session M1: Applications** Session Chair: Minoru Watanabe, Shizuoka University, Japan **FPGA-Based Parallel DBSCAN Architecture** *Neil Scicluna, and Christos-Savvas Bouganis* **FPGA-Based High Performance AES-GCM Using Efficient Karatsuba Ofman Algorithm** *Karim M. Abdellatif, R. Chotin-Avot, and H. Mehrez* **Efficient Elliptic-Curve Cryptography Using Curve25519 on Reconfigurable Devices** *Pascal Sasdrich, and Tim Güneysu* **Accelerating Heap-based Priority Queue in Image Coding Application Using Parallel Index-aware Tree Access** *Yuhui Bai, Syed Zahid Ahmed, and Bertrand Granado*
12:30 - 14:00	**Lunch**

14:00 - 15:20	**Session M2: Methods, Frameworks and OS for Debug, Over-clocking and Relocation** Session Chair: Michael Huebner, Ruhr-University Bochum (RUB), Bochum, Germany **A Unified Framework for Over-Clocking Linear Projections on FPGAs Under PVT Variation** *Rui Policarpo Duarte, and Christos-Savvas Bouganis* **Relocatable Hardware Threads in Run-time Reconfigurable Systems** *Alexander Wold, Andreas Agne, and Jim Torresen* **Faster FPGA Debug: Efficiently Coupling Trace Instruments with User Circuitry** *Eddie Hung, Jeffery B. Goeders, and Steve J.E. Wilton*
15:20 - 15:50	**Coffee Break**
15:50 - 17:10	**Session M3: Memory Architectures** Session Chair: Mazen A. R. Saghir, American University of Beirut (AUB), Lebanon **On the impact of replacing a low-speed memory bus on the Maxeler platform, Using the FPGA's configuration infrastructure** *Karel Heyse, Dirk Stroobandt, Oliver Kadlcek, and Oliver Pell* **Towards Dynamic Cache and Bandwidth Invasion** *Carsten Tradowsky, Martin Schreiber, Malte Vesper, Ivan Domladovec, Maximilian Braun, Hans-Joachim Bungartz, and Jürgen Becker* **Stand-alone Memory Controller for Graphics System** *Tassadaq Hussain, Oscar Palomar, Osman S. Ünsal, Adrian Cristal, Eduard Ayguadé, Mateo Valero, and Amna Haider*
17:10 - 19:30	**Break**
19:30 - 22:30	**Barbecue at the Crowne Plaza Vilamoura Hotel**

Tuesday, April 15

08:15 - 08:40	**Registration**
08:40 - 09:00	**Announcements**
09:00 - 10:00	**Invited Speaker from Industry** **How to achieve IEC61508 Functional Safety and Security with FPGA and ZYNQ; architectures, methods and tools** *Giulio Corradi, Xilinx Inc., Munich, Germany* Chair: Diana Goehringer, Ruhr-University Bochum (RUB), Bochum, Germany
10:00 - 10:45	**Coffee Break and Poster Session #2**

10:45 - 12:30	**Session T1: EU Funded Projects**
	Session Chair: M.D. Santambrogio, Politecnico di Milano, Italy
	DeSyRe: On-demand Adaptive and Recongurable Fault-tolerant SoCs? *I. Sourdis, C. Strydis, A. Armato, C.S. Bouganis, B. Falsa, G.N. Gaydadjiev, S. Isaza, A. Malek, R. Mariani, S. Pagliarini, D. Pnevmatikatos, D.K. Pradhan, G. Rauwerda, R.M. Seepers, R.A. Shak, G. Smaragdos, D.Theodoropoulos, S. Tzilis, and M. Vavouras*
	Effective Reconfigurable Design: the FASTER Approach *D. N. Pnevmatikatos, T. Becker, A. Brokalakis, G. Gaydadjiev, W. Luk, K. Papadimitri-ou, I. Papaefstathiou, O. Pell, C. Pilato, D. Pau, M. D. Santambrogio, D. Sciuto, and D. Stroobandt*
	HARNESS Project: Managing Heterogeneous Computing Resources for a Cloud Platform *José G.F. Coutinho, Oliver Pell, Eoghan O'Neill, Peter Sanders, John McGlone, Paul Grigoras, Wayne Luk and Carmelo Ragusa*
	SAVE: Towards Efficient Resource Management in Heterogeneous System Archi-tectures *G. Durelli, M. Coppola, K. Djafarian, G. Kornaros, A. Miele, M. Paolino, O. Pell, C. Plessl, M.D. Santambrogio, and C. Bolchini*
	Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures *Giuseppe Massari, Edoardo Paone, Michele Scandale, Patrick Bellasi, Gianluca Palermo, Vittorio Zaccaria, Giovanni Agosta, William Fornaciari, and Cristina Silvano*
12:30 - 14:00	**Lunch**
14:00 - 15:20	**Session T2: Methodologies and Tools I**
	Session Chair: Gianluca Palermo, Politecnico di Milano, Italy
	Evaluating High-level Program Invariants Using Reconfigurable Hardware *Joonseok Park, and Pedro Diniz*
	Automated Data Flow Graph partitioning for a hierarchical approach to wordlength optimization *Enrique Sedano, Daniel Menard, and Juan Antonio López*
	Partitioning and Vectorizing Binary Applications for a Reconfigurable Vector Computer *Tobias Kenter, Gavin Vaz, and Christian Plessl*
15:20 - 15:50	**Coffee Break and Poster Session #4**

15:50 - 17:10	**Session T3-A: Remote FPGA Lab Environments** Session Chair: Jose Gabriel de Figueiredo Coutinho, Imperial College of London, UK **Online Learning, Assessment and Prototyping of Digital Systems Using Remote Reconfigurable Computing** *Fearghal Morgan, National University of Ireland, Galway* **eDiViDe: a remote learning platform for FPGA design** *Nele Mentens, Jochen Vandorpe, KU Leuven, Belgium*
15:50 – 18:00	**Session T3-B: ALMA Project Special Session (From Scilab to High Performance Embedded Multicore Systems: The ALMA Approach)** Session Chair: Jürgen Becker, KIT, Germany, Timo Stripf, KIT, Germany **Introducing the ALMA Approach for Compiling Scilab to Multi-Core Architectures** *Jürgen Becker / Timo Stripf, Karlsruhe Institute of Technology, Germany* **Multi-Core Architectures targeted by ALMA Flow** *Kim Sunesen, Recore Systems, The Netherlands* **ADL-based Fine-Grain Optimizations within the ALMA Flow** *Ali El Moussawi, Universite de Rennes I, INRIA Research Institute, France* **Mapping and Scheduling Coarse Grain Hierarchical Task Graphs on Multicore Architectures** *Panayiotis Alefragis, Technological Educational Institute of Western Greece, Greece* **Demonstration of the Integrated ALMA Toolflow** *Timo Stripf, Ali El Moussawi, Panayiotis Alefragis*
18:00 - 19:30	**Break**
19:30 - 22:30	**Gala Dinner at the Hotel**

Wednesday, April 16

08:15 - 08:40	**Registration**
08:40 - 09:00	**Announcements**
09:00 - 10:00	**Invited Speaker from Academia** **Doing Monte-Carlo in 5 micro-seconds: Using FPGAs to go where GPUs can't** *David Thomas, Imperial College London, UK* Chair: Dirk Stroobandt, Ghent University, Belgium
10:00 - 10:45	**Coffee Break and Poster Session #3**

10:45 - 12:05	**Session W1: Architectures** Session Chair: Pedro Diniz, USC Information Sciences Institute, USA **Enhanced radiation tolerance of an optically reconfigurable gate array by exploiting an inversion/ non-inversion implementation** *Takashi Yoza, and Minoru Watanabe* **Hardware-Accelerated Data Compression in Low-Power Wireless Sensor Networks** *Andreas Engel, and Andreas Koch* **OCP2XI Bridge: An OCP to AXI protocol bridge** *Zdravko Panjkov, Juergen Haas, Martin Aigner, Herbert Rosmanith, Tianlun Liu, Roland Poppenreiter, Andreas Wasserbauer, and Richard Hagelauer*
12:05 - 12:30	**Closing Session and Best Paper Award**
12:30 - 14:00	**Lunch**
14:30 - 18:00	**Social Event (A boat cruise through the waters of the Algarve Coast, if the weather allows it)**

Poster Presentations

Poster Session #1: Applications

Monday, April 14: 10:00 - 10:45

Session Chair: Eduardo Marques, ICMC/USP, Brazil

FPGA Implementation of a Video Based Abnormal Action Detection System with Real-time Cubic Higher Order Local Auto-correlation Analysis
Kaoru Hamasaki, Keisuke Dohi, Yuichiro Shibata, and Kiyoshi Oguri

Synthesizable Multicore Platform for Microwave Imaging
Pascal Schleuniger, and Sven Karlsson

An Efficient Implementation of the Adams-Hamilton's Demosaicing Algorithm in FPGAs
Jalal Khalifat, Ali Ebrahim, and Tughrul Arslan

FPGA Design of Delay-Based Digital Effects for Electric Guitar
Pablo Calleja, Gabriel Caffarena, and Ana Iriarte

Design Space Exploration of a Particle Filter Using Higher-order Functions
Rinse Wester, and Jan Kuper

Simulation of Complex Biochemical Pathways in 3D Process Space via Heterogeneous Computing Platform: Preliminary Results
Jie Li, Amin Salighehdar, and Narayan Ganeson

Poster Session #2: Architectures

Tuesday, April 15: 10:00 - 10:45

Session Chair: João Canas Ferreira, University of Porto, Portugal

Efficient Buffer Design and Implementation for Wormhole Routers on FPGAs
Taimour Wehbe, and Xiaofang Wang

MicroACP - A Fast and Secure Reconfigurable Asymmetric Crypto-Processor
Christoph Pöpper, Oliver Mischke, and Tim Güneysu

ARABICA: A Reconfigurable Arithmetic Block for ISA Customization
Ihsen Alouani, Mazen A.R. Saghir, and Smail Niar

Built-in 3-Dimensional Hamming Multiple-Error Correcting Scheme to Mitigate

Radiation Effects in SRAM-Based FPGAs
B. Chagun Basha, Stanislaw J.Piestrak, and Sébastien Pillement

Adapting Processor Grain via Reconfiguration
Jecel Assumpção Jr, Merik Voswinkel, and Eduardo Marques

Instruction Set Optimization for Application Specific Processors
Max Ferger, and Michael Huebner

Poster Session #3: Methodologies and Tools

Wednesday, April 16: 10:00 - 10:45

Session Chair: João Bispo, University of Porto, Portugal

A Dataflow Inspired Programming Paradigm for Coarse-Grained Reconfigurable Arrays
Anja Niedermeier, Jan Kuper, and Gerard J.M. Smit

Thread Shadowing: Using Dynamic Redundancy on Hybrid Multi-cores for Error Detection
Sebastian Meisner, and Marco Platzner

Diffusion-Based Placement Algorithm for Reducing High Interconnect Demand in Congested Regions of FPGAs
Ali Asghar, and Husain Parvez

GPU vs FPGA : A Comparative Analysis for Non-standard Precision
Umar Minhas, Samuel Bayliss, and George A. Constantinides

Instruction Extension and Generation for Adaptive Multicore Processors
Chao Wang, Xi Li, Huizhen Zhang, Liang Shi, and Xuehai Zhou

Poster Session #4: EU-Funded Projects

Tuesday, April 15: 15:20 - 15:50

Session Chair: Marco D. Santambrogio, Politecnico di Milano, Italy

DeSyRe: on-demand Adaptive and Recongurable Fault-tolerant SoCs?
I. Sourdis, C. Strydis, A. Armato, C.S. Bouganis, B. Falsa, G.N. Gaydadjiev, S. Isaza, A. Malek, R. Mariani, S. Pagliarini, D. Pnevmatikatos, D.K. Pradhan, G. Rauwerda, R.M. Seepers, R.A. Shak, G. Smaragdos, D.Theodoropoulos, S. Tzilis, and M. Vavouras

Effective Reconfigurable Design: the FASTER Approach
D. Pnevmatikatos, T. Becker, A. Brokalakis, G. Gaydadjiev, W. Luk, K. Papadimitri-ou, I. Papaefstathiou, O. Pell, C. Pilato, D. Pau, M. D. Santambrogio, D. Sciuto, and D. Stroobandt

HARNESS Project: Managing Heterogeneous Compute Resources for a Cloud Platform
José G.F.Coutinho, Oliver Pell, Eoghan O'Neill, Peter Sanders, John McGlone, Paul Grigoras, Wayne Luk and Carmelo Ragusa

Profile-Guided Compilation of Scilab Algorithms for Multiprocessor Systems
Juergen Becker, Thomas Bruckschloegl, Oliver Oey, Timo Stripf, George Goulas, Nick Raptis, Christos Valouxis, Christos Gogos, Panayiotis Alefragis, Nikolaos S. Voros

SAVE: Towards Efficient Resource Management in Heterogeneous System Archi-tectures
G. Durelli, M. Coppola, K. Djafarian, G. Kornaros, A. Miele, M. Paolino, O. Pell, C. Plessl, M.D. Santambrogio, and C. Bolchini

Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures
Giuseppe Massari, Edoardo Paone, Michele Scandale, Patrick Bellasi, Gianluca Palermo, Vittorio Zaccaria, Giovanni Agosta, William Fornaciari, and Cristina Silvano

Thursday, April 17

08:30 - 10:00	**Hands-on: Online Learning, Assessment and Prototyping of Digital Systems Using Remote Reconfigurable Computing** *Fearghal Morgan, National University of Ireland, Galway*
10:00 - 10:30	**Coffee-Break**
10:30 - 12:30	**Hands-on: eDiViDe: A Remote Learning Platform for FPGA Design** *Nele Mentens, Jochen Vandorpe, KU Leuven, Belgium*

Invited Speakers

Keynote Speaker

Technologies and Platforms for Cyberphysical Systems

Giovanni De Micheli, Professor, IEEE Fellow, ACM Fellow

Institute of Electrical Engineering and of the Integrated Systems Centre, EPF Lausanne, Switzerland

Monday, April 14, 09:00 – 10:00, Room: Sotavento I

Abstract:

Much of our economy and way of living will be affected by nanotechnologies in the decade to come and beyond. Mastering materials at the molecular level and their interaction with living matter opens up unforeseeable horizons. This talk deals with how we will conceive, design and use cyberphysical systems exploiting devices at the edge of the scaling limits. Whereas switching circuits and microelectronics have been the enablers of computer and communication systems, new nano-devices have the potentials to realize innovative computational fabrics whose applications require broader hardware abstractions. Indeed, new electronic devices act as atomic comparators, rather than switches. On this basis, a new flavor of circuit and logic synthesis is possible and effective.

In the second part of my talk I will address scaling of computing systems, and the current trend to manycore systems. Design complexity and usability will depend much on the interconnection schemes among computational elements. The technological feasibility envelope and the related multivariate design optimization problems find solutions in the network-on-chip choice as a general paradigm for circuit core interconnection.

Last I will describe cyberphysical system applications within the frame of the Swiss nano-tera.ch program. I will address the opportunities and limitations of current

computing and communication systems toward addressing problems related to health management and environmental protection.

Short Bio:

Giovanni De Micheli is Professor and Director of the Institute of Electrical Engineering and of the Integrated Systems Centre at EPF Lausanne, Switzerland. He is program leader of the Nano-Tera.ch program. Previously, he was Professor of Electrical Engineering at Stanford University.

He holds a Nuclear Engineer degree (Politecnico di Milano, 1979), a M.S. and a Ph.D. degree in Electrical Engineering and Computer Science (University of California at Berkeley, 1980 and 1983). Prof. De Micheli is a Fellow of ACM and IEEE and a member of the Academia Europaea. His research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis for emerging technologies, networks on chips and 3D integration.

He is also interested in heterogeneous platform design including electrical components and biosensors, as well as in data processing of biomedical information. He is author of: Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994, co-author and/or co-editor of eight other books and of over 500 technical articles. His citation h-index is 81 according to Google Scholar. He is member of the Scientific Advisory Board of IMEC and STMicroelectronics.

Invited Speaker from Industry

How to achieve IEC61508 Functional Safety and Security with FPGA and ZYNQ; architectures, methods and tools

Giulio Corradi, Xilinx Inc., Munich, Germany

Tuesday, April 15, 09:00 – 10:00, Room: Sotavento I

Abstract:

Functional safety applications are in growing demand and Xilinx FPGA technology offers a viable solution especially when significant performances are involved. This paper presents several architectures and methodologies for designing SIL2 and SIL3 applications targeting up hardware fault tolerance HFT=1 based on recent silicon products Series 6, Series 7 and ZYNQ-7000®.

Starting with published FIT values the presentation will explore tools methods, as area partitioning, design preservation, partial reconfiguration, isolation design flow, essential and critical bit masking and faults injection, and related methods to achieve

the desired SIL level. Structural methods will be presented as a mean of testing online the functionality to increase the coverage using internal resources.

System on chip architectures like ZYNQ-7000® offers new options using to implement diverse channels and heterogeneous architectures to mitigate common cause failures will be covered in the paper. The analyzed architectures like lock-step, check pointing and virtualization will be addressed for covering also the application dependent parts. Security breaching is becoming a great concern for industrial product and such threats are now part of the initiator events lists, the paper presents methods, functions and to mitigate those threats.

Short Bio:

Senior System Architect ISM (Industrial Scientific Medical). Responsible for Xilinx about the Industrial architectures, Dr. **Corradi** has 25 years of experience in semiconductors, FPGA, industrial, medical and analytic chemistry applications.

Dr. Corradi current topics of interest are motor control, power systems, power modulation, safety systems around the IEC61508 and safety networking in high performance embedded systems. For Xilinx he is a lead contributor to the IEC61508 and ISO26262 program for SIL3 certification. Before joining Xilinx he designed, managed and supervised several safety related systems in industrial and transportations applications and has been member of the steering group of several EU funded projects, SPIRE, TrainCom, EuroMain and expert in the EU project ModTrain for functional safety. He is active with the IEEE Industrial Electronics Society. Dr. Corradi belongs to the Xilinx ISM (industrial scientific medical) team and he is based in Munich (Germany).

Invited Speaker from Academia

Doing Monte-Carlo in 5 micro-seconds: using FPGAs to go where GPUs can't

David Thomas, Imperial College, London, UK

Wednesday, April 16, 09:00 – 10:00, Room: Sotavento I

Abstract:

In many domains, particularly finance, FPGAs are viewed as a good solution for making low-latency decisions, such as simple message routing and the application of heuristics. For high throughput and batch-oriented numerical tasks it is assumed that GPUs or multi-core CPUs will naturally provide better overall processing power than FPGAs, due to the hardened floating-point units, large-scale parallelism, and high clock-rate. However, FPGAs have the natural advantage that very low-latency pro-

cessing also implies high throughput, providing the best of both worlds.

This talk demonstrates this concept in the context of Monte-Carlo simulation, which is usually seen as a batch-oriented and numerically intensive process suitable for GPUs, and impossible to execute at micro-second time-scales. But we can exploit multiple features of an FPGA architecture to reduce latency, in particular the ability to schedule work and collect results much more quickly than any instruction based architecture. This makes it possible to do a complete numerical Monte-Carlo simulation within 5 micro-seconds (~1000 cycles), a time-scale so small that GPUs can essentially do no computation at all. So because throughput = 1/latency, the same latency-oriented FPGA architecture can also beat the GPU in terms of batch throughput.

Short Bio:

David Thomas received his MEng in software engineering and PhD in hardware acceleration from the Dept. of Computing at Imperial College, and since 2010 has been a lecturer with the Dept. of Electrical and Electronic Engineering. His research has mainly been in the acceleration of computationally intensive applications using FPGAs and GPUs, in fields such as bio-informatics and image processing.

A particular interest is accelerating computational finance using FPGAs, where he performed much of the early academic work in numerical methods for option pricing and risk analysis, which he is now commercialising with BlueBee Technologies. He has won best paper prizes at ARC for his work in hardware accelerated Monte-Carlo simulation, and at FPL for his FPGA-optimised random number generators..

Special Session: EU Funded Projects

April 15 (Tuesday), 10:45 - 12:30, Session T1, Room: Sotavento I

Session Chair: M.D. Santambrogio, Politecnico di Milano, Italy

Invited Talks:

DeSyRe: on-demand Adaptive and Recongurable Fault-tolerant SoCs?

I. Sourdis, C. Strydis, A. Armato, C.S. Bouganis, B. Falsa, G.N. Gaydadjiev, S. Isaza, A. Malek, R. Mariani, S. Pagliarini, D. Pnevmatikatos, D.K. Pradhan, G. Rauwerda, R.M. Seepers, R.A. Shak, G. Smaragdos, D.Theodoropoulos, S. Tzilis, and M. Vavouras

Abstract:

The DeSyRe project builds on-demand adaptive, reliable Systems-on-Chips. In response to the current semiconductor technology trends that make chips becoming less reliable, DeSyRe describes a new generation of by design reliable systems, at a reduced power and performance cost. This is achieved through the following main contributions. DeSyRe defines a fault-tolerant system architecture built out of unreliable components, rather than aiming at totally fault-free and hence more costly chips. In addition, DeSyRe systems are on-demand adaptive to various types and densities of faults, as well as to other system constraints and application requirements. For leveraging on-demand adaptation/customization and reliability at reduced cost, a new dynamically reconfigurable substrate is designed and combined with runtime system software support. The above define a generic and repeatable design framework, which is applied to two medical SoCs with high reliability constraints and diverse performance and power requirements.

One of the main goals of the DeSyRe project is to increase the availability of SoC components in the presence of permanents faults, caused at manufacturing time or due to device aging. A mix of coarse- and fine-grain reconfigurable hardware substrate is designed to isolate and bypass faulty component parts. The flexibility provided by the DeSyRe reconfigurable substrate is exploited at runtime by system op-

timization heuristics, which decide to modify component configuration when a permanent fault is detected, providing graceful degradation.

Short Bio:

Ioannis Sourdis is an Assistant Professor in Computer Engineering at Chalmers University of Technology, Sweden. He has an engineering diploma Dipl-Eng ('02) and a MSc ('04) in electronic and computer engineering from the TU Crete, Greece, and a PhD ('07) in computer engineering from TU Delft, The Netherlands. His research interests include architecture and design of computer and networking systems, reconfigurable computing, interconnection networks and multiprocessor parallel systems, fault-tolerant computing and energy-aware computing.

From 2007 until 2010, Sourdis participated in the coordination of the HiPEAC NoE cluster on Reconfigurable Computing. He has co-authored about 35 papers in Int. conferences and journals, cited in over 800 papers. He is participating in the technical committees of 14 Int. conferences; he is reviewer in 21 Int. journals and more than 30 Int. conferences. Sourdis holds a patent in an address lookup technique for network routing. He participated in the Pro3, EASY, SARC and HiPEAC European projects currently participates in the EMC2 Artemis project, and since 2011 coordinates the DeSyRe FP7 project. He is also member of the HiPEAC NoE, member of the management committee of the MEDIAN Cost Action, member of IEEE and ACM.

Effective Reconfigurable Design: the FASTER Approach

D. Pnevmatikatos, T. Becker, A. Brokalakis, G. Gaydadjiev, W. Luk, **K. Papadimitriou**, I. Papaefstathiou, O. Pell, C. Pilato, D. Pau, M. D. Santambrogio, D. Sciuto, and D. Stroobandt

Abstract:

While fine-grain, reconfigurable devices have been available for years, they are mostly used in a fixed functionality, "asic-replacement" manner. To exploit opportunities for flexible and adaptable run-time exploitation of fine grain reconfigurable resources (as implemented currently in dynamic, partial reconfiguration), better tool support is needed. The FASTER project aims to provide a methodology and a tool-chain that will enable designers to efficiently implement a reconfigurable system on a platform combining software and reconfigurable resources.

Starting from a high-level application description and a target platform, our tools analyse the application, evaluate reconfiguration options, and implement the designer choices on underlying vendor tools. In addition, FASTER addresses micro-reconfiguration, verification, and the run-time management of system resources. We

use industrial applications to demonstrate the effectiveness of the proposed framework and identify new opportunities for reconfigurable technologies.

Short Bio:

Kyprianos Papadimitriou is a Research Associate at the Computer Architecture and VLSI Systems Laboratory of the Institute of Computer Science, FORTH, Crete. He also works as Scientific Staff at the School of ECE of the Technical University of Crete. He received his Diploma and MSc in Electronic and Computer Engineering from the Technical University of Crete, in 1998 and 2003 respectively.

During 1998-1999 he was with the R&D department of ATMEL working on hardware implementation of wireless protocols. In 2003 he co-initiated an effort to establish a spin-off company involved with motion recognition technologies. In 2012 he was granted with a Ph.D from the School of ECE, Technical University of Crete, with a special focus on reconfigurable computing. He is currently working for the FASTER project and has formerly participated in several European and national research projects.

HARNESS Project: Managing Heterogeneous Compute Resources for a Cloud Platform

José G.F. Coutinho, Oliver Pell, Eoghan O'Neill, Peter Sanders, John McGlone, Paul Grigoras, Wayne Luk and Carmelo Ragusa

Abstract:

Most cloud service offerings are based on homogeneous commodity resources, such as large numbers of inexpensive machines interconnected by off-the-shelf networking equipment and disk drives, to provide low-cost application hosting. However, cloud service providers have reached a limit in satisfying performance and cost requirements for important classes of applications, such as geo-exploration and real-time business analytics.

The HARNESS project aims to fill this gap by developing architectural principles that enable the next generation cloud platforms to incorporate heterogeneous technologies such as reconfigurable Dataflow Engines (DFEs), programmable routers, and SSDs, and provide as a result vastly increased performance, reduced energy consumption, and lower cost profiles. In this paper we focus on three challenges for supporting heterogeneous computing resources in the context of a cloud platform, namely: (1) cross-optimisation of heterogeneous computing resources, (2) resource virtualisation and (3) programming heterogeneous platforms.

Short Bio:

Jose G.F. Coutinho is an associate researcher working in the Custom Computing Re-

search Group at Imperial College London. He received his M.Eng. degree in Computer Engineering from Instituto Superior Tecnico, Lisbon, Portugal in 1997. From 2000 and 2007 he received his M.Sc. and PhD in Computing Science from Imperial College London. Since 2005, he has been involved in UK and EU research projects such as Ubisense, hArtes, REFLECT and HARNESS. His main interests include mapping and optimising high-level descriptions to heterogeneous reconfigurable platforms and aspect-oriented design. He has published over 40 research papers in peer-referred journals and international conferences and has contributed to two book publications.

SAVE - Towards Efficient Resource Management in Heterogeneous System Architectures

G. Durelli, M. Coppola, K. Djafarian, G. Kornaros, A. Miele, M. Paolino, O. Pell, C. Plessl, M.D. Santambrogio, and C. Bolchini

Abstract:

The increasing availability of different kinds of processing resources in heterogeneous system architectures associated with today's fast-changing, unpredictable workloads has propelled an interest towards systems able to dynamically and autonomously adapt how computing resources are exploited to optimize a given goal. Self-adaptiveness and hardware-assisted virtualization are the two key-enabling technologies for this kind of architectures, to allow the efficient exploitation of the available resources based on the current working context.

The SAVE project will develop HW/SW/OS components that allow for deciding at runtime the mapping of the computation kernels on the appropriate type of resource, based on the current system context and requirements.

Short Bio:

Gianluca Durelli received his Bachelor and Master of Science in Computer Engineering from the Politecnico di Milano respectively in September 2009 and April 2012. He is currently in his second year of Ph.D. in Computer Science at the Politecnico di Milano and his research focuses on self-adaptive systems for heterogeneous computing platforms.

During his first year as a Ph.D. student he did an internship at IBM T.J. Watson Research Center working in the High Performance Analytics group.

Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures

G. Massari, E. Paone, M. Scandale, P. Bellasi, **G. Palermo**, V. Zaccaria, G. Agosta, W. Fornaciari, C. Silvano

Abstract:

Since the silicon technology entered the many-core era, new computing platforms are exploiting higher and higher levels of parallelism. Thanks to scalable, clustered architectures, embedded systems and high-performance computing (HPC) are rapidly converging. We are also experiencing a rapid overlapping of the challenges related to efficient exploitation of processing resources. Platform-specific optimization and application boosting cannot be considered independently anymore. Thus the increased interest towards broader and versatile methodologies, which could easily scale from the embedded up to the general-purpose domain. [...] This paper proposes an innovative methodology, defined during the 2PARMA project, based on a properly defined run-time support to enable an effective exploitation of design-time information. The synergy between design-time and run-time provides an efficient yet portable run-time management solution which could scale from embedded to general purpose systems. The methodology proposes the integration of independent tools to provide effective compilation of OpenCL code, multi-objective design space exploration, system-wide run-time resource management and application-specific monitoring and tuning [...].

Short Bio:

Gianluca Palermo received the M.S degree in Electronic Engineering, in 2002, and the Ph.D degree in Computer Engineering, in 2006, from Politecnico di Milano. He is currently an assistant professor at Department of Electronics and Information Technology in the same University. Previously he was also consultant engineer in the Low Power Design Group of AST - STMicroelectronics working on network on-chip and research assistant at the Advanced Learning and Research Institute (ALaRI) of the Università della Svizzera italiana (Switzerland).

He has actively participated in several EU-research projects. Since 2003, he published over 100 research papers in international conferences and journals. His research interests include design methodologies and architectures for multi-core embedded system.

Special Session: ALMA Project

April 15 (Tuesday), 15:50 - 18:00, Session T3-B, Room: Sotavento 1

Session Chairs**: Jürgen Becker**, **Timo Stripf**, Karlsruhe Institute of Technology, Germany

15:50 - 16:20

Introducing the ALMA Approach for Compiling Scilab to Multi-Core Architectures

Jürgen Becker, Timo Stripf, Karlsruhe Institute of Technology, Germany

Short Bio:

Jürgen Becker is Full Professor for Embedded Electronic Systems in the department of Electrical Engineering and Information Technology at Universität Karlsruhe (TH). His actual research is focused on industrial-driven System-on-Chip (SoC) integration with emphasis on heterogeneous multi-core architecture solutions with high performance issues and safety features. This includes also online adaptivity, e.g. dynamically reconfigurable hardware technologies.

Primary applications are automotive, industrial automation and communication systems. Prof. Becker is Head of the Institute for Information Processing (ITIV) and Department Director of Electronic Systems and Microsystems (ESM) at the Computer Science Research Center (FZI). From 2001 - 2005 he has been Co-Director of the International Department at Universität Karlsruhe (TH), and from 2002 - 2008 Associate Editor of the IEEE Transactions on Computers.

He is author and co-author of more than 400 scientific papers, and active as general and technical program chairman of national / international conferences and workshops. He is executive board member of the German IEEE section, Board member of the GI/ITG Technical Committee of Architectures for VLSI Circuits, and Senior Member of the IEEE. Since October 2005 Prof. Becker has been Board Member and Vice-President ("Prorektor") for Studies and Teaching at Universität Karlsruhe (TH), and from October 2009 - April 2012 Chief Higher Education Officer (CHEO) in the new

Karlsruhe Institute of Technology - KIT. Since July 2012 Prof. Becker is Secretary General of CLUSTER - the association of 12 leading European technical universities. In May 2013 Juergen Becker received the honorary doctor (Dr. h. c.) from Technical University of Budapest.

16:20 - 16:45

Multi-Core Architectures targeted by ALMA Flow

Gerard Rauwerda, Recore Systems, The Netherlands

Short Bio:

Gerard Rauwerda is CTO and co-founder at Recore Systems. He has a background in electrical engineering, and a PhD in heterogeneous many-core SoCs for adaptive wireless communications systems. His interests lie in fault-tolerant many-core data processing platforms and programmer-friendly efficient parallel programming of many-core systems.

16:45 - 17:10

ADL-based Fine-Grain Optimizations within the ALMA Flow

Ali El Moussawi, Universite de Rennes I, INRIA Research Institute, France

Short Bio:

Ali Hassan El Moussawi is a Ph.D. student at University of Rennes 1. He received a Master's degree in Computer Science from University of Paris IV, and worked as an intern in Texas Instruments France (2012). He is currently working on source-to-source compiling techniques. His research interests include Polyhedral Model, SIMD vectorization and Floating-to-Fix point conversion.

17:10 - 17:35

Mapping and Scheduling Coarse Grain Hierarchical Task Graphs on Multi-core Architectures

Panayiotis Alefragis, Technological Educational Institute of Western Greece, Greece

Short Bio:

Prof. **Panayiotis Alefragis** has more than 18 years of experience in software engineering and the design of optimization algorithms for very large scale problems in various application areas. He has coauthored over 40 articles in refereed scientific journals & conference proceedings and he has extensive practical experience by participating in various national and international research projects in the above areas.

His research interests include software engineering, parallel/distributed computing and systems, grid computing, programming languages and compilers, business rules modeling, resource scheduling algorithms, algorithm engineering, integer and combinatorial optimization, wireless / mobile network applications and embedded design optimization.

Prof. Alefragis was one of the founders and the Managing Director of Lyseis Ltd, a specialized software company for optimization software for the airline industry, with clients including, among others, Lufthansa AG and AIMS.He is currently faculty of the Computers and Informatics Engineering Department of the TEI of Western Greece. Prof. Alefragis holds a Diploma and a PhD in Electrical & Computer Engineering from University of Patras. He is a member of the IEEE and the Engineering Chamber of Greece. He can be contacted by sending an e-mail at alefrag at teimes.gr.

17:35 - 18:00:

Demonstration of the Integrated ALMA Toolflow

Timo Stripf, Ali El Moussawi, Panayiotis Alefragis

Short Bio:

Timo Stripf is a Post-Doc student in the research group of Jürgen Becker in the department of Electrical Engineering and Information Technology (ITIV) at Karlsruhe Institute of Technology (KIT). He received his diploma in computer science in 2007 and successfully passed his PhD defense in 2013. He has participated in the 4S and MORPHEUS European project as well as the KAHRISMA national funded project.

He is currently coordinating the ALMA European Project. His research interests are architecture description languages (ADL) for processor core and MPSoCs, superscalar and VLIW processor architecture design, compiler toolchains for VLIW processors, ADL-based SystemC simulation and Matlab to C compilation..

Special Session and Tutorial: Remote FPGA Labs

Special Session (Session T3-A): April 15 (Tuesday), 15:50 - 17:10, Room: Sotavento 2

Tutorials: April 17 (Thursday), 08:30 - 12:30, Room: Sotavento 1

April 15 (Tuesday), 15:50 - 17:10, Room: Sotavento 2

Online Learning, Assessment and Prototyping of Digital Systems using Remote Reconfigurable Computing

Fearghal Morgan, National University of Ireland, Galway, Ireland

Abstract:

Engineering design is best learnt through practical hands-on experience. The presentation will illustrate Vicilogic, a self-paced, directed training, assessment and proto-typing platform for digital systems using a scalable array of remote FPGAs. The presentation will report on the use of Vicilogic in teaching since 2011. Visually probe inside remote FPGA hardware through animated web-based block diagrams, timing diagrams, state machines and truth tables. During the presentation, ARC attendees will be able to interact with the array of remote FPGAs and experience new methods for Reconfigurable Computing education. The presentation will describe the Vicilogic architecture and demonstrate the Vicilogic course builder, design animation creator and assessment tools which enable tutor creation of online teaching material.

Short Bio:

Fearghal Morgan leads the Bio-Inspired Electronics and Reconfigurable Computing Research Group, National University of Ireland Galway (NUI Galway). Fearghal has 20 years teaching and research experience and 7 years design industry experience. He holds a B.Sc. (Hons) and Ph.D. in Electrical and Electronic Engineering, Queen's University Belfast (1981 and 1986).

Recent and current research projects include the Enterprise Ireland funded Vicilogic project, NUI Galway PI on the Si elegans FP7 project (http://www.si-elegans.eu/), and

collaborator on the Science Foundation Ireland "Efficient Embedded DSP Research Cluster".

eDiViDe: a remote learning platform for FPGA design

Nele Mentens, Jochen Vandorpe, KU Leuven, Belgium

Abstract:

eDiViDe (European Digital Virtual Design lab) is a European project funded by LLP-Erasmus funding of the EACEA and by OOF funding of the KU Leuven. The platform consists of many FPGA-driven setups that are locally hosted by universities in at least five different countries and remotely connected to a central server in Belgium. All setups are available through www.edivide.eu. Students can upload their VHDL-code to the remotely accessible FPGAs and evaluate the results of their design through video and/or audio feedback. This way, students can practice their digital design skills anytime and anywhere (given they have access to the internet through a browser). Further, the setups are related to the expertise of the participating research groups, which results in a motivating and inspiring learning environment. Besides practicing digital design skills through exercises at all levels, from beginner to expert, the platform also allows researchers to cooperate remotely. Finally, the platform can also be interesting for companies for recruiting or training purposes.

Short Bios:

Nele Mentens obtained a Ph.D. in Engineering Science at KU Leuven in 2007. Her research interests are in the field of cryptographic coprocessors in secure embedded systems, dynamically reconfigurable hardware for security purposes, EDA for cryptographic hardware/software and remote FPGA labs. Currently, she is an assistant professor at KU Leuven, Campus Diepenbeek, where she founded the research group "Embedded Systems & Security" in 2008. Nele is also part of the COSIC group at KU Leuven.

Jochen Vandorpe obtained a Master degree in Industrial Engineering in 2005 at KU Leuven, Campus Diepenbeek. He spent 6 years in industry, working on mobile telecommunications products and networking solutions in mainly international environments. He joined the Embedded Systems & Security group at KU Leuven, Campus Diepenbeek in 2011, where he is responsible for the eDiViDe project.

Tutorials: Thursday, April 17, 8:30-12:30, Room: Sotavento I

08:30 - 10:00 Hands-on: Online Learning, Assessment and Prototyping of Digital Systems using Remote Reconfigurable Computing

Speaker: **Fearghal Morgan**, National University of Ireland, Galway

Tutorial:

The goal of the tutorial is to enable each attendee to:

1. Understand the principles of Vicilogic by following a short online directed learning and assessment lesson using remote FPGAs. The lesson will provide hands-on directed learning of combinational and sequential components, with animated block diagrams, timing diagrams, state machines and truth tables. A sandbox will enable user control and interaction with the lesson examples. Automatic assessment will capture user understanding.
2. Build your own application and control/visualisation console using Vicilogic. Users can bring along their own VHDL-based project component example, captured and simulated using Xilinx EDA toolsuite (Vivado or PlanAhead) and associated diagrams graphically describing the design and/or its state machine(s). Each attendee will follow an automated process to wrap their VHDL design for execution on Vicilogic, generate a Vicilogic FPGA configuration file (using Xilinx tools installed on their laptop), upload the configuration file and design diagrams to Vicilogic, and build an animated console enabling real-time control and visualisation of the design executing on a remote FPGA.
3. Build their own lesson using Vicilogic Users will apply the course builder to develop a short lesson which includes their project example.

Attendees should bring a laptop, with Xilinx Vivado or PlanAhead EDA tools installed and licensed. Wireless access and Vicilogic registration will be provided.

Contact fearghal.morgan@nuigalway.ie for further information.

10:00 - 10:30 Coffee-Break

10:30 - 12:30 Hands-on: eDiViDe: a remote learning platform for FPGA design

Speakers: **Nele Mentens, Jochen Vandorpe**, KU Leuven, Belgium

Tutorial:

The target audience of the workshop are professors and teaching/research assistants that are interested in using the platform for their courses/research. Both the use of

the platform and the option to extend the platform with a new locally hosted, remotely connected setup are explained during the workshop. Company representatives that are interested in using the platform for training or recruitment purposes are also encouraged to participate in the workshop.

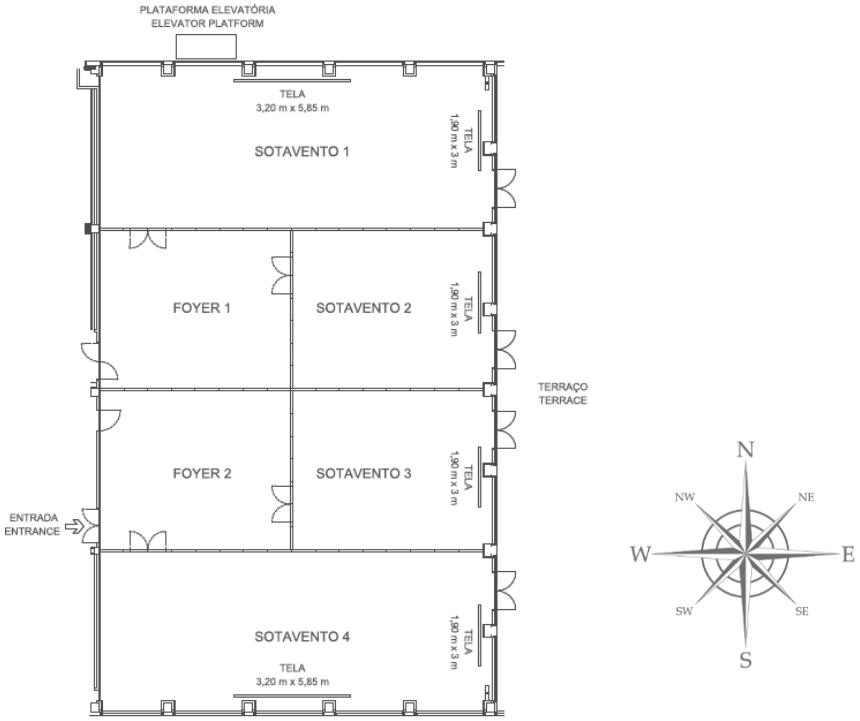
All participants are requested to bring their own laptop with a firefox or chrome browser.

Conference Area

The main area for the conference is at the first floor of the Crowne Plaza Hotel. The rooms for the conference presentations are **Sotavento 1**, and **Sotavento 2**. The exhibition, poster sessions and the coffee-breaks will run at room **Sotavento 4**.

Below is a table that summarizes the locations of the main conference activities and a map of the conference area.

Space for:	Location in the Crown Plaza Hotel
Presentation rooms	Rooms **Sotavento 1** and **Sotavento 2**
Coffee-Breaks, Poster Sessions, and Exhibition	**Sotavento 4**
Conference Secretariat	Room **Sotavento 3**
Welcome Cocktail	**Sea Front** or **Caravela Bar** (depending on the weather)
Lunches (Chef's Buffet)	**Cataplana Restaurant**
Gala Dinner	**Banquetes room**
BBQ (barbeque)	**Sea Front** or **Banquetes room** (depending on the weather)



Social Events

Welcome Cocktail

Sunday, April 13, 2014

Location: Crowne Plaza Vilamoura Hotel, "Caravela Seafront " or "Caravela Bar" (depending on the weather)

Schedule: 18:00-19:30

19:00-19:30 Versus Tuna - Tuna Académica da Universidade do Algarve

Barbeque

Monday, April 14, 2014

Location: Crowne Plaza Vilamoura Hotel, "Caravela Seafront" or "Banquetes" Room (depending on the weather)

Schedule: 19:30 - 22:30

21:00-22:00 Music by "Rosa dos Ventos" (José Luís Argain e Inês Rosa) (Portuguese Pop Music and Bossa Nova)

Gala Dinner

Tuesday, April 15, 2014

Location: Crowne Plaza Vilamoura Hotel, "Banquetes" Room

Schedule: 19:30 - 22:30

21:30-22:00 Music by João Frade (Accordion, Instrumental, World Music)

Algarve Coast Boat Cruise[1]

Wednesday, April 16, Afternoon, 2014

Meeting Point: Crowne Plaza Hotel Reception at 14:15

Boat: "Condor de Vilamoura"

Schedule: 14:30 to 18:00

Description:

The trip: a 3 hour coastal cruise. Leaving Vilamoura Marina head west along the coast passing Praia da Oura, Albufeira and viewing some of the caves and rock for-

[1] The boat cruise is dependent of the weather conditions.

mations to the beach of Galé. We will stop for a swim in the summertime. On morning cruises in the summer there will be a cave visit, sea condition permitting. Return to Vilamoura.

The Condor: A replica of a 2 mast American fishing scooner from the 1825-1935 period. The Condor is docked at: Quay I #25, at Vilamoura Marine (in front of the Marinotel).

Practical Information

Wi-Fi Access (free)

Coverage	All hotel area
Access information	**Network Name:** Crowne Plaza **Username:** arc **Password:** 2014

Conference Office

Department of Informatics Engineering, Faculty of Engineering, University of Porto, Secretariat: (+351) 22 508 2134

Service Numbers

Emergency Service Numbers / Ambulance Emergency Service

SOS - Número Nacional de Socorro - 112

Police/Emergency call

Guarda Nacional Républicana (GNR): (+351) 289381780

GNR QUARTEIRA: (+351) 289310420 ♦ GNR VILAMOURA: LOULÉ: (+351) 289410490

Fire service/rescue control center

BOMBEIROS LOULÉ: (+351) 289400560

Taxis

ROTÁXI (Vilamoura): (+351) 289 895799 ♦ ROTÁXI (Faro): (+351) 289 895790

Transport Faro Airport ↔ Crown Plaza hotel

By taxi:

There are taxis all day and night at the airport, prices vary between 30 and 45 EUR, from Faro airport to Vilamoura.

Taxis can be called using phone numbers +351 289 30 01 60 / +351 289 31 56 50 or taken at the taxi rank located near the hotel. Maximum capacity is 4 persons. Expect 30 EUR for a one way trip from Vilamoura to Faro.

By Bus:

Leaving from Faro Airport take bus no. 14 (towards “Atalaia”) or bus no. 16 (towards “Terminal Rodoviário”). Exit the bus at the “Terminal Rodoviário”, and take bus towards Vilamoura (P. Marina).

Conference Venue

This year's ARC symposium will be held at the Crowne Plaza Vilamoura Hotel, a privileged location in the well-known destination of Vilamoura and only 20 minutes away from the Faro International Airport.

The Algarve, with an average of 300 days of sunshine a year, is the most popular and cosmopolitan region of Portugal, with a wealth of natural and man-made attractions, from superb beaches and dramatic scenery to some of the best golf courses and marinas in Europe.

The hotel features a large garden area, an outdoor swimming pool with approximately 1000m^2, the Almond Tree Wellness Spa with treatment rooms, Hammam and dry Sauna, indoor heated pool and large whirlpool and a Fitness Center with state of the art equipment; a multipurpose field for tennis, football, etc.; a putting green for improve golfers short game and the Peter Pan Kids Club for our little guests.

Crowne Plaza Vilamoura - Algarve Hotel & Spa
Rua do Oceano Atlântico
8126-913 Vilamoura - Algarve Portugal
GPS: 37° 4'22.74"N / 8° 6'52.52"W
Phone: (+351) 289 381 600
Fax: (+351) 289 381 652

http://www.crowneplazavilamoura.com/

Notes:

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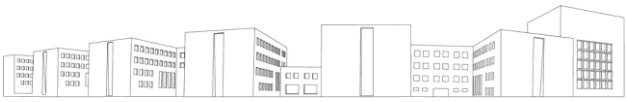

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